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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
4717-11400

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	First Named Inventor Bruno Ghyselen	
	Art Unit 2812	Examiner L. Schillinger

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

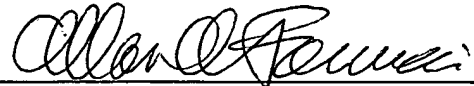
I am the

☐ applicant/inventor.

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See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
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☒ attorney or agent of record. **30,256**
Registration number _____

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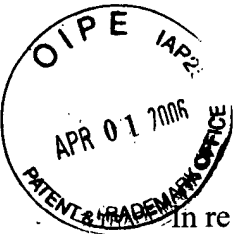

Signature
Allan A. Fanucci, Reg. No. 30.256
Typed or printed name
212-294-3311
Telephone number
March 31, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Bruno GHYSELEN et al.

Confirmation No. 7267

Application No: 10/686,082

Group Art Unit: 2812

Filing Date: October 14, 2003

Examiner: L. Schillinger

For: PREVENTIVE TREATMENT METHOD
FOR A MULTILAYER SEMICONDUCTOR
STRUCTURE

Atty. Docket No.: 4717-11400

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF

Commissioner for Patents

P.O. Box 1450

Alexandria, Virginia 22313-1450

Sir:

Applicants request a panel review of the decision of the Examiner mailed January 10, 2006 rejecting claims 1, 3-7 and 9-20.

In the final office action, claims 1, 3-7 and 9-19 were again rejected as being anticipated by US patent 6,902,987 to Tong et al. ("Tong"). Applicants submit that this rejection is in error and are seeking further review by appeal.

The independent claims define a method for preparing a multilayer semiconductor structure wherein a protective layer is formed between an intermediate insulating layer and a surface layer of the structure. This protective layer protects the insulating layer from the subsequent chemical treatments to which the structure is exposed after the structure is formed. The structure is formed by bonding a donor substrate to the support substrate; and then transferring at least the surface layer from the donor substrate to the support substrate by a layer transfer technique to form the multilayer structure. Then, the surface layer of that structure can be chemically treated, e.g., with hydrofluoric acid, without attacking the insulating layer due to the presence of the protecting layer.

Tong discloses a method for bonding surfaces at low temperature by etching first and second bonding surfaces before bonding them together at room temperature. The etching is used to roughen the surfaces so that different materials can be bonded together. The surface roughness may be in a range of 0.1 to 3 nm. The preparation of the surfaces (see Figs. 1 and 2) consists of (1) forming bonding layers (col. 5 lines 6-15); (2) conducting an etching step to improve planarity and roughness (col. 5 lines 31-40); (3) polishing layer surfaces (col. 5 lines 16-30), further etching to activate the bonding layer surfaces (by VSE : Very Slight Etch, Plasma, RIE ...) (col. 5 line 41 to col. 6 line 19), conducting a post VSE process by immersing the wafers in a chemical solution to terminate the surfaces (col. 6 lines 30-57), and then, bonding the surfaces together at room temperature (col. 6 line 59 to col. 8 line 22).

Tong thus discloses a method for bonding two wafer surfaces at room temperature wherein different chemical treatments are used during the preparation of the wafer surfaces and prior to bonding. Fig. 3C is referenced in office action (point 1), but this does not disclose the present invention, because Fig. 3 shows a structure having a bonding layer 32 having a free face, and a layer 31. If one considers the structure disclosed by Tong in Fig. 3C, in combination with the disclosure at col. 5 lines 35-40, a silicon nitride layer can be inserted inside the bonding layer 32. This means that a silicon nitride layer will divide the bonding layer 32 in two parts: 1) the upper bonding layer 32 which has a free face and could be considered to be the equivalent of the surface layer of the present invention.; and 2) the lower portion of the bonding layer 32 which could be assimilated to the intermediate layer 2 of the present invention.

According to this interpretation, a number of significant differences are seen for applicants' invention, including that the surface layer of Tong, which is a bonding layer of an insulating material, is not protected by a protective layer. Tong "protects" the rear or non-exposed surface of the layer with the silicon nitride layer. To use Tong as a teaching of the presently claimed invention, a skilled artisan would find that Tong's bonding layer is "protecting" the silicon nitride layer, and this is the opposite to what is claimed. Tong's bonding layer is not made of a protective material as he clearly discloses that the layer is etched to provide enhanced bonding properties. In contrast, the present claims recite the protection of a thin layer of a semiconductor material by a layer of a protecting material that is provided between the thin layer and the intermediate insulating layer. This structure is not taught or disclosed by any possible reading of Tong.

Furthermore, the composition of the surface and intermediate layers disclosed by Tong are different. Tong's surface layer and intermediate layer have the same composition, (see Fig. 3C) while in the present invention, the surface layer material is a semiconductor material while the intermediate buried layer is an insulating layer. Consequently, as the surface layer 32 of Tong has the same composition as the intermediate layer, it certainly will be etched by a chemical solution that etches the surface layer. In fact, Tong's invention requires that the material be etched to improve bonding so he certainly would not use a protective material to prevent etching as that would negate what he is teaching as a benefit by providing such a surface layer. Thus, Tong's surface layer is not made from a material chosen to be sufficiently resistant to the chemical treatment to protect the intermediate layer from chemical attack, as recited in current claims 1 and 20. Thus, Tong does not disclose or inherently result in the presently claimed invention.

In col. 5 lines 31-40, Tong discloses that the etching and polishing are realized directly on the bonding layer 32 to improve the roughness of that surface. The use of a silicon nitride layer as a protective layer is suggested to limit the attack of the SiO₂ bonding layer 32 by the HF that is applied during the smoothing step. In contrast, in the present invention, the semiconductor surface layer is not eliminated with the chemical treatment used to attack the intermediate insulating layer [0026], [0033], since this chemical attack is performed after manufacturing of the full structure (surface layer, intermediate layer, protection layer) and the protective layer prevents further attack beyond the surface layer.

Therefore, the silicon nitride layer disclosed in the Tong is used to prepare the bonding layer before bonding the wafers to form the final structure, rather than to protect subjacent layers in the final structure as in the present invention.. In the present invention, this protective layer prevents attack of the buried insulating layer by the chemical treatments occurring after the fabrication of the final substrate, and of course after the bonding step (Figs. 5 to 9 and [0010] of the published application). And nowhere in Tong is it suggested or disclosed that a chemical treatment realized after the bonding step, on the surface layer of the bonded structure, could lead to defects in the intermediate layer that could be prevented by the provision of a protective layer.

The comments on the last page of the office action seem to be directed to different claims than the ones that are currently of record. Each of the claim recitations that are relied

upon for patentability are certainly present in claims 1 and 20. Thus, a hearing is requested so that applicants can discuss these differences and demonstrate why they support the novelty and unobviousness of the present claims.

3-31-06
Date

Respectfully submitted,


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